WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory blocks;

signal lines respectively connected to said plurality of memory blocks; and

a control circuit connected to said signal lines, said control circuit including selection signal generator circuits for generating selection signals for selecting one memory block of said plurality of memory blocks by externally input address signals and for outputting said selection signals to said signal lines,

wherein lengths of the signal lines from said selection signal generator circuits to the respective memory blocks are longer in proportion to distances from said control circuit to said memory blocks.

2. A semiconductor memory device according to Claim 1, wherein driving capabilities of said selection signal generator circuits are larger in proportion to the distances from said control circuit to said memory blocks.

3. A semiconductor memory device according to Claim 2, wherein differences between driving capabilities of said selection signal generator circuits for outputting said selection signals to said signal lines are determined by ratios of lengths of said signal lines connected to said control circuit.

4. A semiconductor memory device according to Claim 1, wherein

gate widths of transistors that constitute said selection signal generator circuits are longer in proportion to the distances from said control circuit to said memory blocks.

5. A semiconductor memory device according to Claim 4, wherein differences between the gate widths of transistors that constitute said selection signal generator circuits for outputting said selection signals to the respective signal lines are determined by ratios of lengths of said signal lines connected to said control circuit.

6. A semiconductor memory device according to Claim 1, wherein said selection signal generator circuits are constituted by NAND circuits with said address signals as input.

7. A semiconductor memory device according to Claim 1, wherein said control circuit further includes a signal driver circuit for transmitting said selection signals to the respective memory blocks.

8. A semiconductor memory device according to Claim 7, wherein driving capability of said signal driver circuit is larger in proportion to the distances from said control circuit to said memory blocks.

9. A semiconductor memory device according to Claim 7, wherein gate widths of transistors that constitute said signal driver circuit are longer in proportion to the distances from said control circuit to said memory blocks.

10. A semiconductor memory device according to Claim 7, wherein

said signal driver circuit is constituted by inverters with output of said selection signal generator circuits as input.

11. A semiconductor memory device comprising:

a plurality of memory blocks disposed along a first direction;

signal lines respectively connected to said plurality of memory blocks; and

a control circuit disposed apart from said plurality of memory cells along said first direction and connected to said signal lines, said control circuit including selection signal generator circuits for generating selection signals for selecting one memory block of said plurality of memory blocks by externally input address signals and for outputting said selection signals to said signal lines,

wherein lengths of said signal lines from said selection signal generator circuits to the respective memory blocks are longer in proportion to distances from said control circuit to said memory blocks.